LISTING OF THE CLAIMS:

Claims 1-26 (cancelled).

27. (New) A component comprising a chip having component structures, said chip comprising, on one surface, solderable metallizations connected with the component structures, a carrier substrate having, on a lower surface, contacts for electrically conductive connection with the component structures of the chip, conductor traces extending from the contact to connection areas, wherein the connection areas are respectively at least partially uncovered on a floor of recesses in the carrier substrate, said chip being mounted in a flip-chip arrangement by means of bump connections arranged in the recesses, said bump connections electrically-conductively connecting the solderable metallizations of the chip to the connection areas of the carrier substrate, so that the chip at least partially rests on the carrier substrate.

28. (New) A component according to claim 27, wherein the carrier substrate is a multi-layer carrier substrate having at least an upper layer and a lower layer and wherein the connection areas are arranged on the surface of the lower layer.

29. (New) A component according to claim 27, wherein the contacts on the lower surface of the carrier substrate are arranged below recesses in the carrier substrate.

30. (New) A component according to claim 27, wherein the chip is fashioned on a piezoelectric substrate to form a component selected from a group consisting of SAW components, FBAR resonator, BAW resonator and SCF filter.

31. (New) A component according to claim 30, wherein one of the chip and carrier substrate is provided with a frame so that a part of the component structure is arranged in a hollow that is enclosed by the frame and both the surface of the chip and the surface of the carrier substrate facing the chip, in that the frame forms a support for one of the chip and the carrier substrate and in that the contact

area between the carrier substrate and chip is circumferentially sealed with a closed solder border.

32. (New) A component according to claim 31, wherein the frame is formed from a material selected from plastic or metallization on one of the surfaces of the chip and carrier substrate or is the boundary of a depression provided on the surface of the carrier substrate, said depression having a depth which corresponds at least to the height of the component structure arranged in the hollow.

33. (New) A component according to claim 31, wherein the frame is fashioned as a metallization on the surface of the carrier substrate and is arranged circumferentially along and underneath the chip edge facing the carrier substrate and in that the boundary surface between the frame and chip is circumferentially sealed with a closed solder border.

34. (New) A component according to claim 27, wherein the carrier substrate is a multi-layer carrier substrate having at least two layers with a lower layer being provided with feedthroughs that are filled with a conductive material, the surface of the feedthroughs forming the connection area of the substrate.

35. (New) A component according to claim 27, wherein the carrier substrate is a low-warpage LTCC ceramic.

36. (New) A component according to claim 27, wherein the carrier substrate is a multi-layer substrate having at least two layers, said metallized contacts being provided on the underside of a lower layer of the multi-layer carrier substrate and being connected by feedthroughs with the wiring arranged between the two layers of the at least two-layer carrier substrate, with the wirings being selected as the connection areas or being connected to the connection areas.

37. (New) A component according to claim 27, wherein the chip is metallized at least in the region of its lower edge and the carrier substrate is metallized at least on a band below the lower edge of the chip, whereby the

metallization comprises at least one of the metals selected from a group consisting of Al, Ni, Cu, Pt and Au.

38. (New) A component according to claim 27, wherein the chip, on a back side, has a lacquer layer selectively removed to generate an inscription for the chip.

39. (New) A component according to claim 38, wherein additional layers forming an optical contrast with the lacquer layer are provided under the lacquer layer of the chip.

40. (New) A component according to claim 27, wherein the outer edges of the chip are canted and taper toward the carrier substrate.

41. (New) A method for producing an encapsulated component, said method comprising the steps of providing a multi-layer carrier substrate which comprises recesses of a depth h1 in which solderable connection areas are uncovered, providing a chip having component structures on one surface as well as solderable metallizations connected with said component structures, generating a depression having a depth h2 for acceptance of the component structure of the height h3 on one of the surface of the chip and the carrier structure, creating solder bumps on one of the solderable connection areas and solderable metallizations having a height h4, whereby h4>(h1+h2), attaching the chip to the carrier substrate with a flip-chip arrangement by melting the soldered bumps so that the solder connection areas are connected via the solder bumps with the solderable metallization and upon a mutual shrinking of the solder bumps conditional upon melting, the chip height drops to (h1+h2) on the carrier substrate and rests there, whereby the component structures are arranged in a hollow of the height h2 formed by the depression and covered by the chip and carrier substrate.

42. (New) A method according to claim 41, wherein the first contact metallizations are created on the carrier substrate in the region below the lower chip edge, the second contact metallizations being generated on the chip in the region

between the contact barrier and the facing chip area, and a solder border circling the chip being created for connection of the first and second contact metallizations.

43. (New) A method according to claim 41, wherein the chip narrowing toward the surface with the contact structures with canted side edges is used, the solder border being generated on the carrier substrate before the attachment of the chip in that soldering the side edges of the chip are attached with the metallizations located there to the solder borders and are soldered therewith.

44. (New) A method according to claim 41, wherein the step of creating the solder bumps generates the solder bumps on a solderable metallization of the chip and the solderable connection areas of the carrier substrate by a method selected from a group consisting of galvanic deposition, silk screen, stencil printing, scraping of solder paste into recesses of the carrier substrate, vibration of solder balls into the recesses of the carrier substrate, laser bumping and stamping of solder foil over the recesses.

45. (New) A method according to claim 41, wherein the carrier substrate is a multiple carrier substrate having at least an upper layer and a lower layer, the recesses are created in the upper layer and filled with conductive material, the solderable connecting areas being a solder coating on a surface of the lower layer facing the upper layer under the recesses of the upper layer.

46. (New) A method according to claim 45, wherein the base of the recesses is selected larger in the upper layer than the area of the solderable connection areas on the surface of the lower layer in that the cross-section of the bumps is selected smaller than those of the recesses.

47. (New) A method according to claim 41, wherein, after the step of soldering and generating the solder border, material is removed from the back side of the chip by a method selected from particle beam removal and abrasion, so that the chip is thinned.

48. (New) A method according to claim 41, wherein the chips are being applied to a large-area carrier substrate and are first subsequently isolated into components or modules via a division of the carrier substrate between the chips.

49. (New) A method according to claim 48, wherein the isolation occurs via a beam method in which the solder border serves as a mask.

50. (New) A method according to claim 41, wherein the step of providing the multi-layer carrier substrate provides a multi-layer of green ceramic, forming recesses in the upper layer of the multi-layer green ceramic, filling the recesses with a filling material and then sintering the multi-layer green ceramic to form multi-layer sintered ceramics and then removing the filling material after sintering.

51. (New) A method according to claim 50, wherein the step of filling the recesses and removal of the filling material again is selected from a group consisting of filling with Al_2O_3 and removing the Al_2O_3 with a beam process; filling with a PbO and removing the PbO via dissolution with an acetic acid and filling with a carbon-containing material and removing the carbon-containing material via dissolving with acetic acid.

52. (New) A method according to claim 41, wherein the step of bonding the bumps to the solderable metallizations is improved by following a step selected from roughening the chip surface before the application of the metallizations in the region of the solderable metallizations and structured application of the metallizations so that an open band-like, grid-like or sieve-like structure of the solderable metallizations is created, in whose openings the chip is uncovered.